DOUBLE-INJECTION, DEEP-IMPURITY SWITCH DEVELOPMENT

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16. Abstract

The overall objective of this program is the development of device design and process techniques for the fabrication of a double-injection, deep-impurity $(DI)^2$ silicon switch that operates in the 1-10 kV range with conduction current of 10 and 1A, respectively. Other major specifications include a holding voltage of 0 to 5 volts at 1 A anode current, 10 microsecond switching time, and power dissipation of 50 W at 75°C.

This report describes work that shows how the results obtained at the University of Cincinnati under NASA Grant NSG-3022 have been applied to larger area and higher voltage devices. The investigations include theoretical, analytical, and experimental studies of device design and processing. Methods to introduce deep levels, such as Au diffusion and electron irradiation, have been carried out to "pin down" the Fermi level and control device-switching characteristics. Different anode, cathode, and gate configurations are presented. Techniques to control the surface electric field of planar structures used for $(DI)^2$ switches are examined.

Various sections of this report describe the device design, wafer-processing techniques, and various measurements which include ac and dc characteristics, 4-point probe, and spreading resistance.

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1. SUMMARY

The overall objective of this program is the development of device design and process techniques for the fabrication of a double-injection, deep-impurity [$(DI)^2$] silicon switch that operates in the 1-10 kV range with conduction current values of 10 and 1 A, respectively. Other major specifications include a holding voltage of 0 to 5 volts at 1 A anode current, 10 μsec switching time, and power dissipation of 50 W at 75°C.

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2. INTRODUCTION

Double injection in semi-insulators is of considerable interest because of the unique current-voltage characteristics which can be put into practical use in high-voltage switching applications. Double injection has been exclusively referred to as the simultaneous injection of both electrons and holes from n- and p-type electrodes, respectively, into the semi-insulating region. They are essentially p-i-n diodes.

Double injection into insulators and semi-insulators in which carrier trapping is present has been treated theoretically,[1,2,3] and some experimental investigations have been made for devices fabricated from semi-insulating Si and other semiconductor materials.[3,4,5]

Of particular interest is the case resulting from the introduction of deep-lying energy levels in the intrinsic region. These devices, referred to as deep-impurity and double-injection or $(DI)^2$ devices, give rise to current-controlled negative resistance (CCNR) under proper conditions of doping and bias.

Planar configuration $(DI)^2$ devices (Figure 1) are of greatest interest for their IC process compatibility and gating convenience. These devices exhibit an s-type switching behavior similar to the one shown in Figure 2.

The threshold voltage, V_T, for the onset of the Negative Differential Resistance (DNR) and the corresponding holding voltage, V_H, subsequent to the NDR regime can be simply expressed as[6]:

$$V_{TH} = N_t \, v_p \, \sigma_p \, \frac{L^2}{\mu_p} \qquad (1)$$

$$V_H = N_t \, v_n \, \sigma_n \, \frac{L^2}{\mu_p} \qquad (2)$$

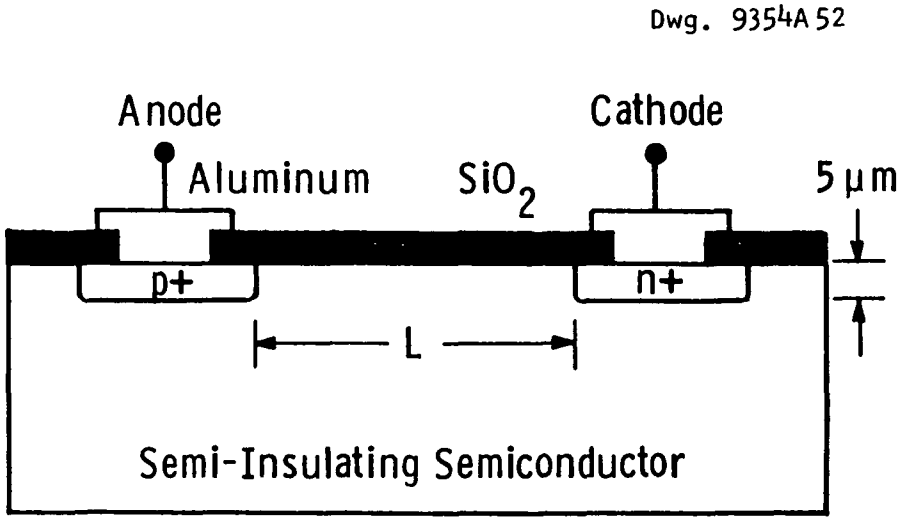

Figure 1. Cross section of a $(DI)^2$ planar device.

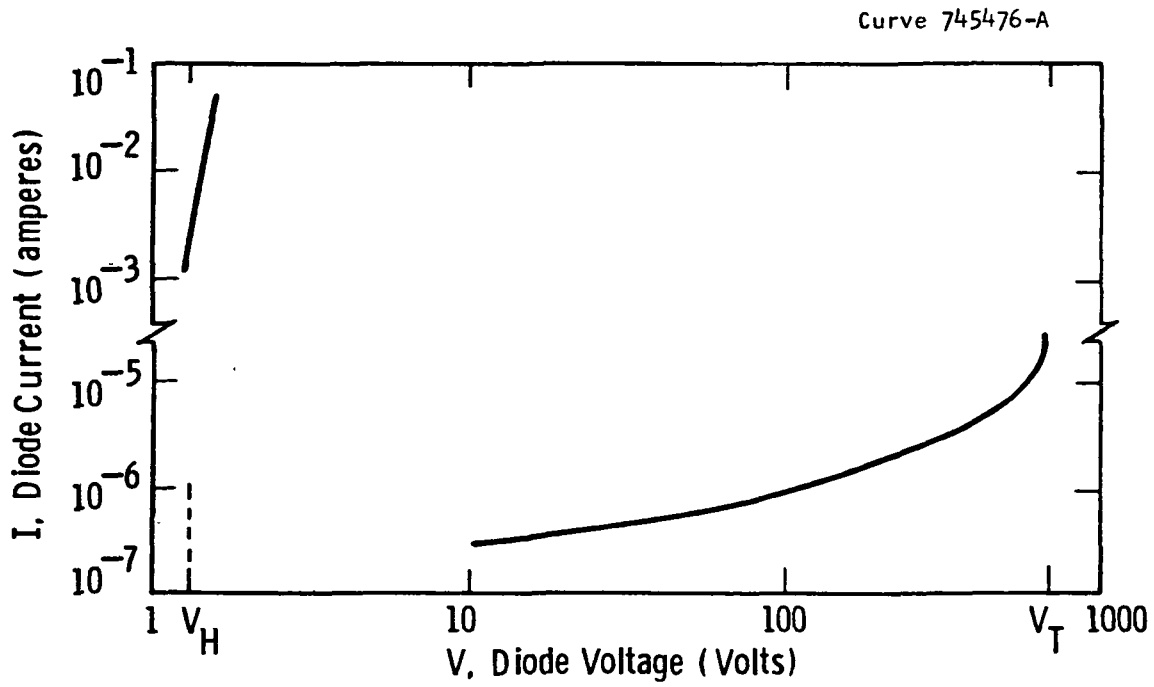

Figure 2. I-V characteristics of $(DI)^2$ device.

where, μ_p = hole mobility

v_n, v_p = thermal velocity of electrons and holes, respectively

N_t = trap concentration

L = device channel length (Figure 1)

Efforts have been made to maximize the threshold voltage (V_T) and minimize the corresponding holding voltage (V_H) of these devices for power-switching applications.

This report describes work that shows how the results obtained at the University of Cincinnati under a NASA grant have been extended to higher voltage and higher current devices. Rather than simply scaling up mask dimensions, a number of new ideas and modifications have been made. These include:

1. Circular concentric anode/cathode planar configurations with or without MOS gates.
2. Vertical symmetric rectangular electrodes with different electrode surface areas.
3. Lateral rectangular electrodes with different anode/cathode electrode spacing.
4. Electron irradiation and Co diffusion as well as Au diffusion for creation of deep-energy levels in Si.
5. Field plate and SIPOS termination for control of surface field.

Various sections of this report describe the design, processing, electrical measurements, and analysis of these new device structures. The report concludes with various projections and recommendations for future work.

3. DEVICE DESIGN

3.1 Background

As is true in many situations, the design of the $(DI)^2$ switch requires a compromise. The requirement for the device to achieve a high threshold voltage, V_{TH}, conflicts with the need to have a low holding voltage, V_H. This is apparent from Equations 1 and 2:

$$\frac{V_H}{V_{TH}} = \frac{v_n \sigma_n}{v_p \sigma_p} \tag{3}$$

The challenge would be, then, to find the energy level and doping for the lowest electron-capture cross section and highest hole-capture cross section to minimize V_H/V_{TH}. At the same time, the surface electric field has to be controlled to achieve bulk breakdown voltages, while the contribution of contact resistance to holding voltage is minimized. Moreover, carrier injection and gate triggering have to be optimized for I-V control.

3.2 Mask Design

Two different mask sets were obtained from the University of Cincinnati. One mask set is a symmetrical rectangular anode/cathode configuration without a gate. The other set is an asymmetrical configuration with a separate guard ring diffusion. The guard ring diffusion is carried out with the cathode diffusion.

New mask sets which incorporate a number of features that improve the overall performance have been designed. These features are:

1. Planar circular concentric anode/cathode configurations with symmetric electrodes (Figure 3). One design has no gate and the

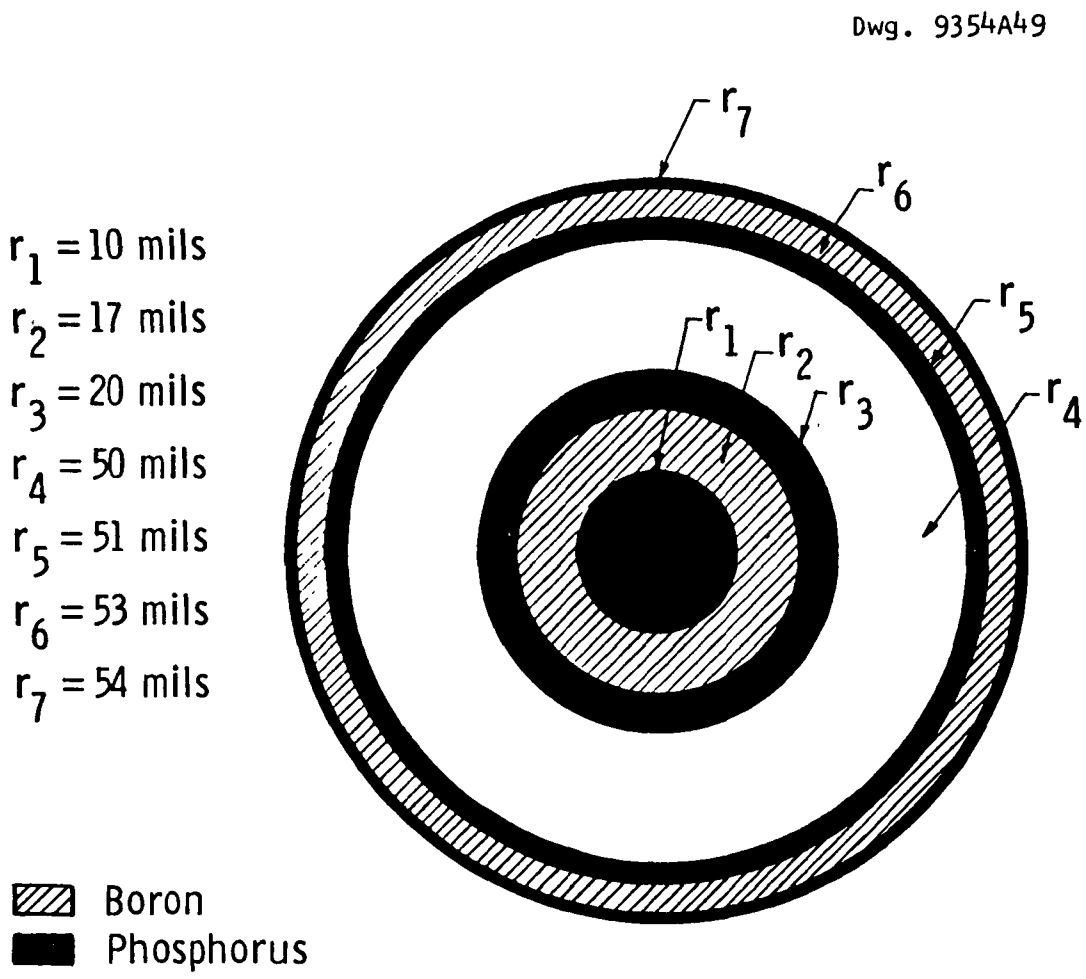

Figure 3. Planar concentric anode/cathode $(DI)^2$ device with symmetric electrodes.

other design has a MOS gate with the spacing between electrode and gate of 5, 10, and 15 mils. A similar configuration has been employed before at Westinghouse for high-voltage planar devices.[7]

2. Vertical double-alignment symmetric electrodes (Figure 4). Four different electrode surface areas have been investigated. These are: a) 25×10^{-4} cm^2, b) 100×10^{-4} cm^2, c) 225×10^{-4} cm^2, and d) 400×10^{-4} cm^2.
3. Planar devices that have rectangular electrodes with spacings of 5, 10, 15, 20, and 25 mils to study the effect of anode/cathode electrode spacing on threshold voltage, V_T. There are both injection gates and MOS gates. The electrodes have different surface areas and are symmetrical (Figure 5).

In addition to the above device masks, test pattern masks have been designed to check the gettering effects of phosphorus and boron on Au and Co.

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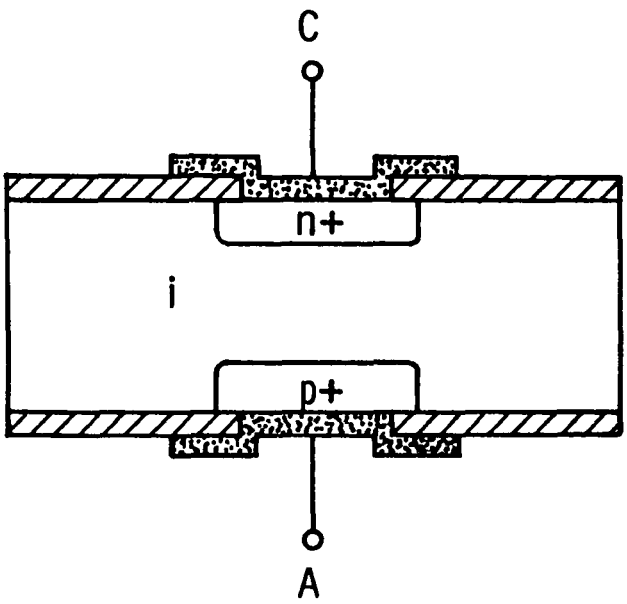

Figure 4. Vertical PIN $(DI)^2$ switch.

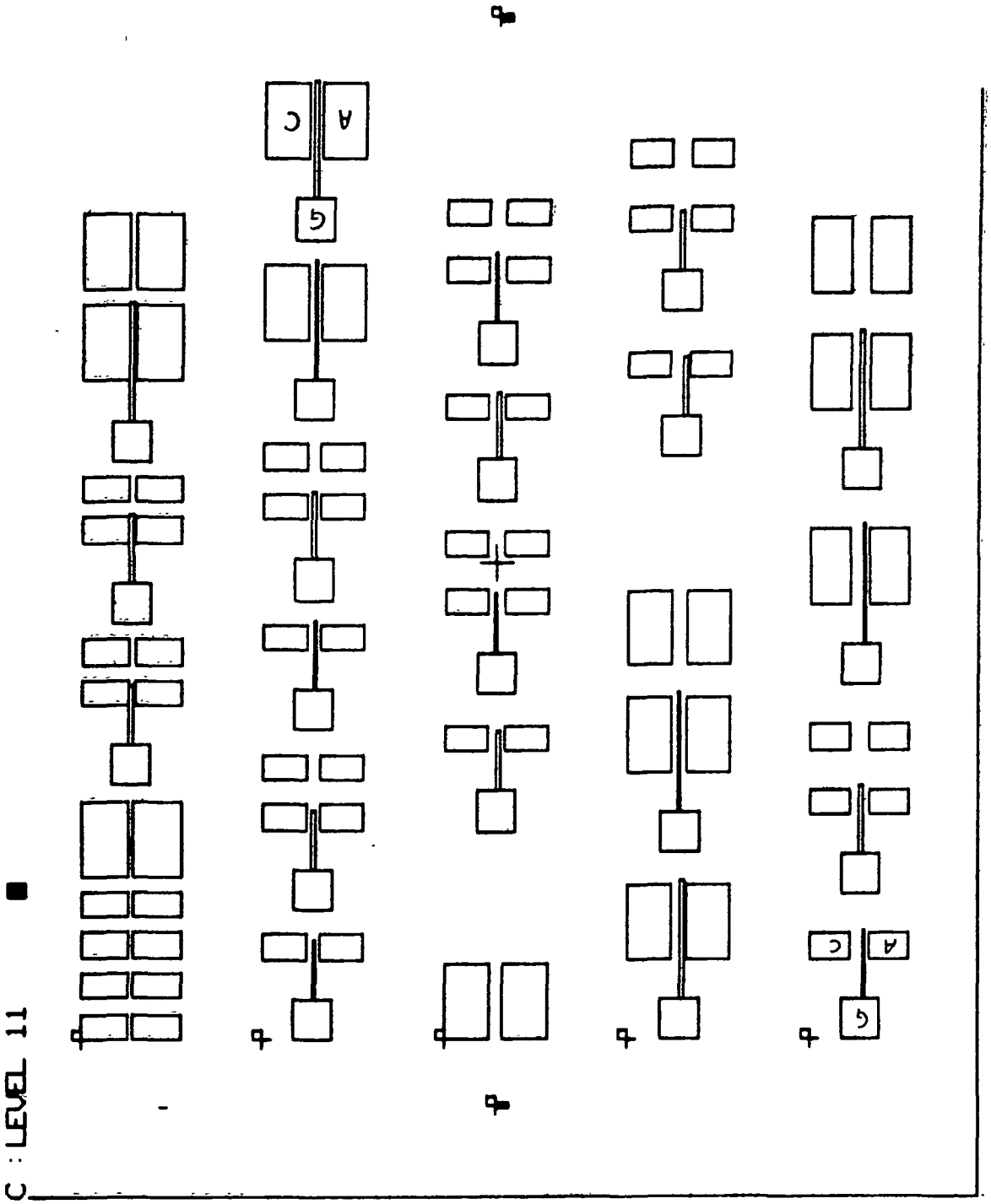

Figure 5. Layout of planar rectangular $(DI)^2$ devices with and without gates.

4. RESULTS

4.1 Device Fabrication

A processing flow diagram indicating the various steps and appropriate device cross section is shown in Figure 6. Most of the steps involve conventional silicon-processing procedures. Gated devices are processed with the injection gate diffused at the same time with the anode p^+ electrode, or with the MOS gate involving no diffusion, as shown in Figure 7.

A completed processed wafer with many devices is shown in Figure 8.

4.2 Gold Diffusion

Diffusion of gold into Si has been performed using a spin-on indirect method developed at the University of Cincinnati. Gold silica was applied onto a source Si wafer which is then used as a Au source during the device Au diffusion process.

Table 1 shows change in resistivity after a one-hour Au diffusion into n-type Si at 1100°C. Spreading resistance and 4-point probe measurement techniques were used.

To study the optimum Au diffusion temperature and time cycle, diffusion was carried out at different temperatures into Si with different starting resistivities. Figures 9 and 10 show spreading resistance profile results for diffusion temperatures of 950, 1000, 1050, 1100, and 1138°C into Si with 10 and 100 ohm-cm starting resistivity.

It is apparent from Figures 9 and 10 that a flat profile is obtained at 1100°C for both 10 and 100 ohm-cm resistivities. The diffusion was performed on Si test wafers without n^+ and p^+ electrode

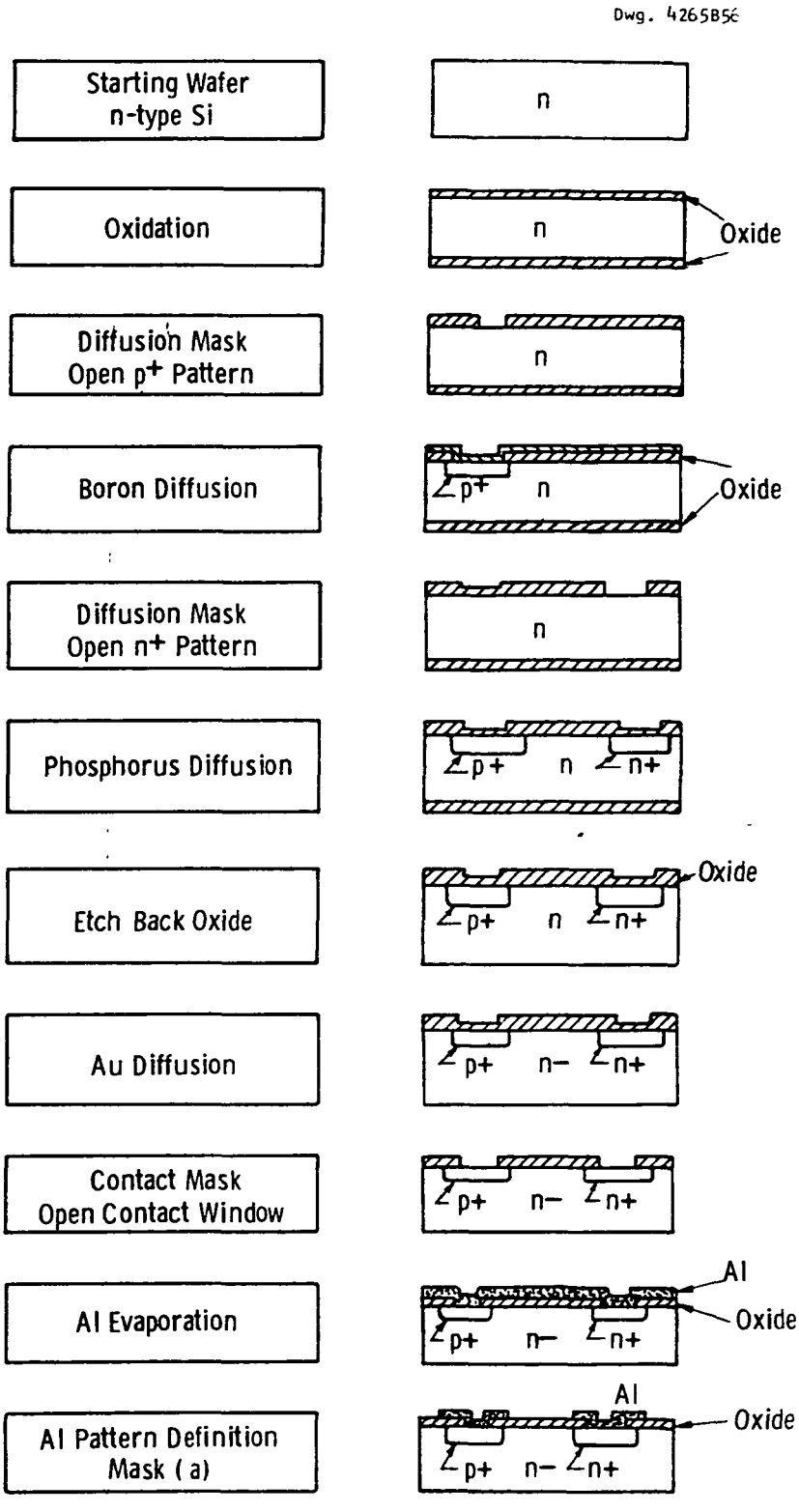

Figure 6. Processing flow sheet with device cross section.

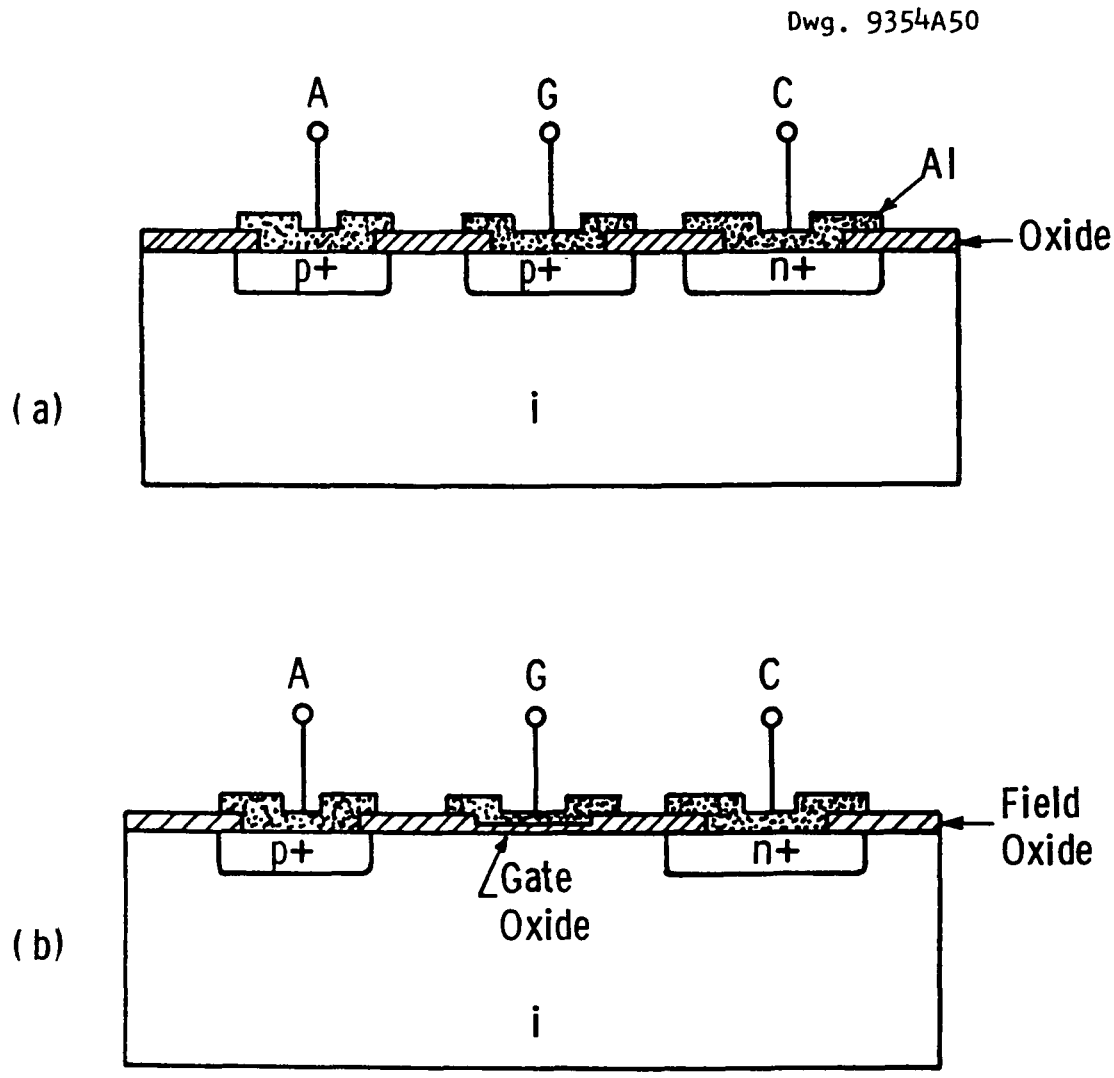

Figure 7. Cross section of $(DI)^2$ devices with n^+ injection gate or MOS gate.

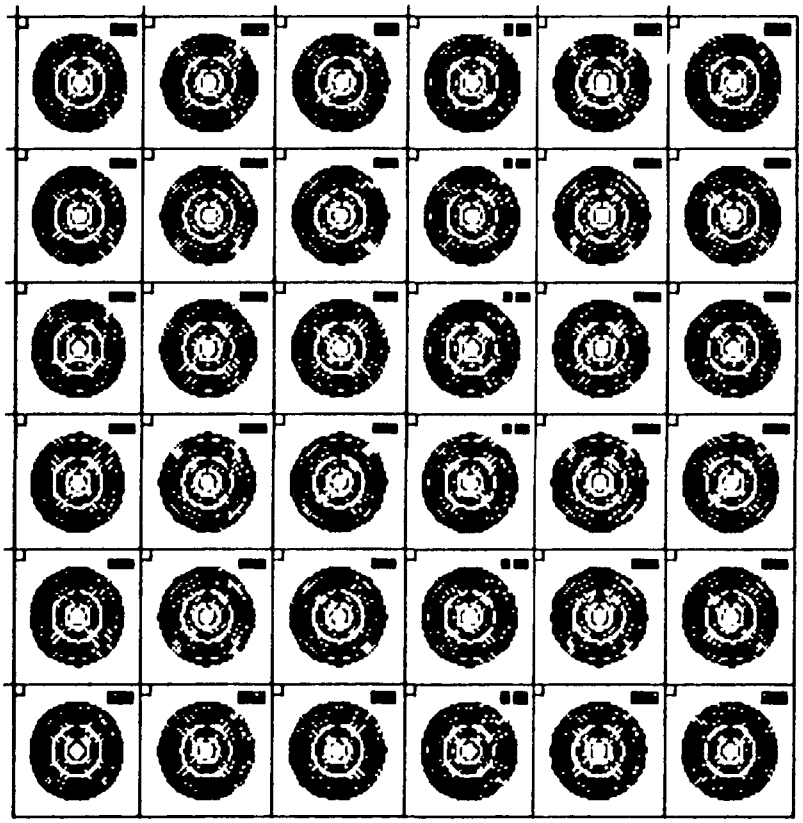

Figure 8. A completed processed $(DI)^2$ wafer.

Table 1

Gold Diffusion in Si at 1100°C for One Hour
(2-inch diameter, 11.5 → 12.0 mil <111>, n-type)

	R E S I S T I V I T Y			
	4-Point Probe		Spreading Resistance	
Sample Number	Before Diffusion	After Diffusion	Before Diffusion	After Diffusion
1	9.8 Ω-cm	2.4×10^4 Ω-cm	10 Ω-cm	5.5×10^3 Ω-cm
2	9.1	2.6×10^4	9.5	5.3×10^3
3	6.2	$.81 \times 10^4$	6.4	4.5×10^3
4	8.2	1.02×10^4	10	4.0×10^3

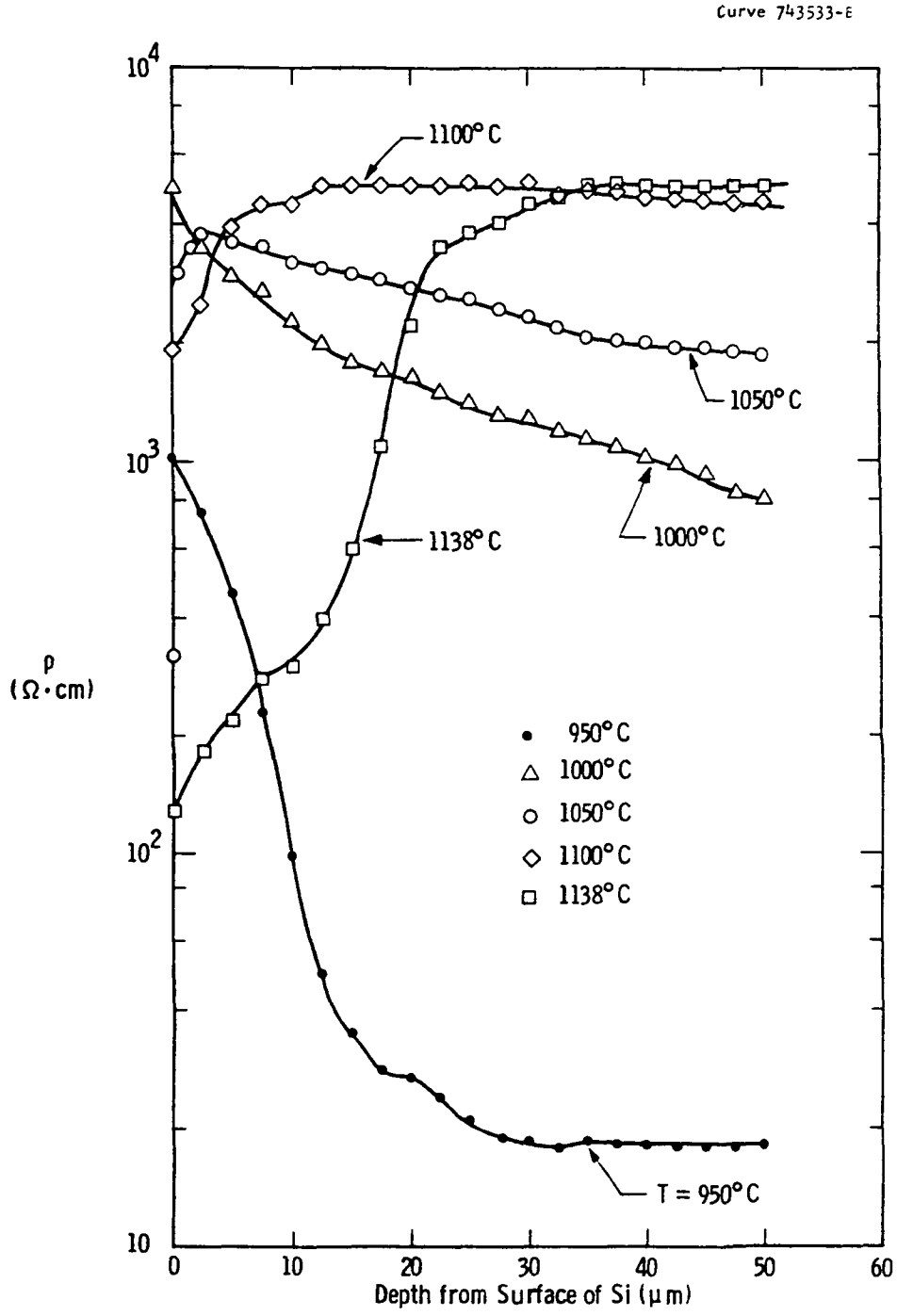

Figure 9. Spreading resistance measurement of Si wafers that have been Au doped at temperatures (950°C → 1138°C) for one hour using an indirect source; starting material is n-type, 10 ohm-cm Si.

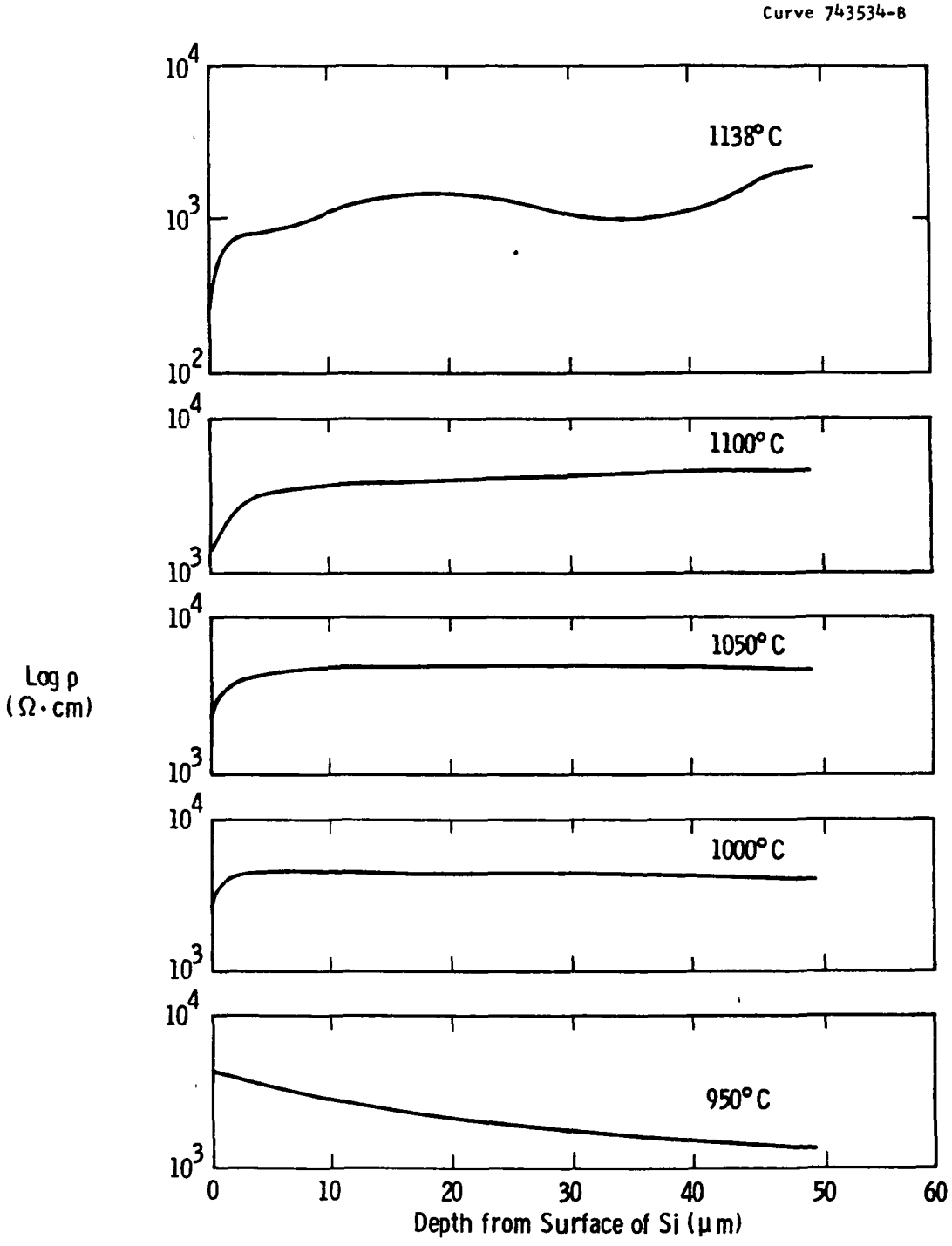

Figure 10. Spreading resistance measurement of Si wafers that have been Au doped at temperatures (950°C → 1138°C) for one hour using an indirect source; starting material is n-type, 100 ohm-cm Si.

processing. It is expected that different profiles will be obtained when Au diffusion is performed on device wafers after electrode processing. This is due to the gettering effects of the n^+ phosphorus electrode. It is believed that gold atoms diffusing through the back surface of the device will be gettered toward the highly phosphorus-doped diffusion on the front side. This will result in a nonuniform diffusion profile with higher Au concentration under the diffused electrodes. Nevertheless, it has been found that a uniform gold concentration profile along the device channel does not give the best switching characteristics.[8] This is because the deep traps near the cathode provide more contribution to the blocking voltage than do the traps near the anode. Moreover, the deep traps near the anode tend to increase the holding voltage after the device switches on. Therefore, the graded profile caused by gold gettering toward the n^+ electrode may improve the device switching characteristics.

4.3 Electron Irradiation

An alternate means of introducing deep centers in Si is by electron bombardment. The deep centers result from defects created in the lattice by the bombarding electrons.[9] The most attractive feature of the technique is the ability to tailor the device characteristics after complete fabrication without disturbing the p and n diffusion doping profile. Moreover, no gettering effect is encountered during this process. However, electron irradiation introduces several deep centers,[10,11] and it is difficult to establish the effectiveness or contribution of the various centers in controlling the switching characteristics of $(DI)^2$ devices.

We have measured the effect of different doses of electron irradiation on Si wafers of different starting resistivities. Table 2 shows resistivity results using 4-point probe and spreading resistance measurement techniques. Due to the difficulties associated with high-resistivity measurements using these techniques, these results are indicative of the changes in resistivity values. The device electrical

Table 2

The Effect of Different Doses of Electron Irradiation on the Resistivity of Silicon of Different Starting Resistivities. (All samples are n-type with <111> orientation.)

Electron Dosage	Starting Resistivity	4 Pt. Probe	Spreading Resistance
10^{16} $\frac{\text{electrons}}{\text{cm}^2}$	10 Ω-cm	14 Ω-cm	11.5 Ω-cm
10^{17}	10	2,300	300
10^{18}	10	26,000	700
10^{15}	100	1,600	441
10^{16}	100	19,000	>10,000
10^{17}	100	1,600	270
10^{14}	1,300	2,300	1,569
10^{15}	1,300	21,000	8,006
10^{16}	1,300	75,000	>10,000

measurements corresponding to these electron irradiation results are discussed below.

4.4 Device Test and Analysis

Table 3 shows a summary of the results obtained for the circular lateral devices with deep levels introduced by Au diffusion. The threshold voltage, V_T, holding voltage, V_H, and resistance in the Ohm's Law regime blocking region, R_B, are measured before and after Al sintering. A high threshold voltage of 1350 V with a holding voltage of 50 V is shown for devices with Si starting resistivity of 10 ohm-cm after Au diffusion at 1100°C and before Al sintering. However, this threshold voltage deteriorated upon Al sintering at 450°C. Similar results were obtained for other Au-diffusion temperatures and Si starting resistivities. This can be explained as due to change in surface-state density, which may be contributing to the shift in device current-voltage characteristics. The surface-state density is expected to change after Al sintering at 450°C.

A shift in the I-V characteristics in the direction of increased current was also observed with increased field and time. This phenomenon is illustrated in Figure 11. The shift in current-voltage characteristics was recovered with decreasing field, an effect which can be attributed to heating or carrier trapping.

Similar effects were observed for electron-irradiation lateral circular devices. Table 4 shows current-voltage characteristic parameters, i.e., V_T, V_H, and R_B, as a function of electron irradiation dose. It is interesting to observe inversion from n-type to p-type conductivity with increasing electron dosage level, an effect we have also observed in neutron transmutation doping of Si.[12]

For the vertical "sandwich" devices the same inversion effect was also observed. Tables 5, 6, and 7 show I-V results with electron irradiation. The effect of the electrode area is noted in Table 8. It is

Table 3

Circular Lateral Devices That Have Been Gold Diffused
(The electrode spacing is 760 μm [∼30 mil].)

Starting Resistivity	Al Sinter 450°C	Gold Diffusion Temperature	V_T	V_H	V_T/V_H	R_B
10 Ω-cm	No	1050°C	850 V	70 V	12	400 KΩ
10 Ω-cm	Yes	1050°C	450 V	50 V	9	70 KΩ
10 Ω-cm	No	1100°C	1350 V	50 V	27	2.5 MΩ
10 Ω-cm	Yes	1100°C	670 V	50 V	13.4	70 KΩ
100 Ω-cm	No	950°C	450 V	100 V	4.5	∼ 2 MΩ
100 Ω-cm	Yes	950°C	200 V	120 V	1.7	-
100 Ω-cm	No	1000°C	320 V	60 V	5.3	∼ 2 MΩ
100 Ω-cm	Yes	1000°C	300 V	150 V	2	-

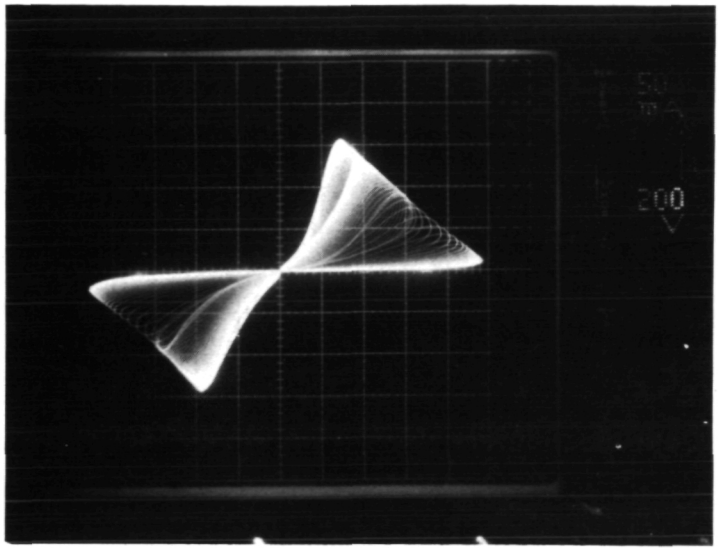

Figure 11. Current-voltage characteristics, in ac mode, showing shift in the direction of increasing current and decreasing voltage.

Table 4

Circular Lateral Devices That Have Been Irradiated With 2MeV Electrons
(The electrode spacing is 760 μm [∿30 mil].)

Dose	Starting Resistivity	V_T	V_H	V_T/V_H	R_B	Test Piece	ρ	Type
None	10 Ω-cm	8.0 V	-	-	45 Ω	Ir-TS-14	15.4 Ω-cm	n
10^{16} cm^{-2}	10 Ω-cm	†	-	-	91 Ω	Ir-TS-14	43	*
6.7 x 10^{16}	10 Ω-cm	180 V	110 V	1.6	4.4 KΩ	Ir-TS-14	9,800	n
None	100 Ω-cm	∿10 V	-	-	300 Ω	Ir-TS-100	104	n
10^{15} cm^{-2}	100 Ω-cm	520 V	100 V	5.2	12.5 KΩ	Ir-TS-100	12,700	*
6.7 x 10^{16}	100 Ω-cm	500 V	50 V	10	50 KΩ	Ir-TS-100	89,000	p

† Curve was linear.

* Didn't measure.

Table 5

Vertical Devices Made From 1300 Ω-cm Material Irradiated With 2 MeV Electron At a Dosage Level of 6.7×10^{16} cm^{-2} (The measurements have been made on the smallest electrodes [500 μm x 500 μm] and V_H is taken at 400 mA)

Sample	Thickness	V_T	V_H	V_T/V_H	R_B
2-2	10 mil	250 V	50 V	5	∿ 400 K Ω
2-6	20 mil	600 V	80 V	7.5	∿ 400 K Ω
2-9	40 mil	1250 V	180 V	6.9	∿ 400 K Ω

Table 6

Vertical Devices Made from 1300 Ω-cm Material Irradiated With 2 MeV Electron At a Dosage Level of 6.7×10^{16} cm^{-2} (The measurements have been made on the largest electrodes [2000 μm x 2000 μm] and V_H is taken at 400 mA)

Sample	Thickness	V_T	V_H	V_T/V_H	R_B
2-2	10 mil	300 V	40 V	7.5	∿ 300 K Ω
2-6	20 mil	480 V	80 V	6.0	∿ 300 K Ω
2-9	40 mil	750 V	200 V	3.75	∿ 400 K Ω

Table 7

Vertical Devices Made From 1300 Ω-cm Material 40 mil Thick and Irradiated With 2 MeV Electrons (The measurements have been made on the smallest electrodes [500 μm x 500 μm] and V_H is taken at 400 mA.)

Dose	Sample	V_T	V_H	V_T/V_H	R_B	Test Piece	ρ	Type
None	1-8	4.8 V	2.5 V	1.9	4 KΩ	VT-1	1300 Ω-cm	n
None	2-9	6.2 V	1.8 V	3.4	6 K	VT-2	1420	n
10^{14} cm^{-2}						14	2900	n
10^{15}	1-8	∿200 V	∿190 V	1.1	∿ 1 KΩ	15	54000	n
10^{16}	1-8	520 V	160 V	3.3	10 KΩ	VT-2	50000	*
10^{16}	2-9	700 V	160 V	4.4	50 KΩ	16	73000	p
5×10^{16}	1-8	1040 V	160 V	6.5	∿300 KΩ			
6.7×10^{16}	2-9	1250 V	180 V	6.9	400 KΩ	VT-2	80000	p
10^{17}	1-8	1500 V	200 V	7.5	∿400 Ω	VT-1	36000	p

*didn't measure it.

Table 8

Vertical Devices Made From 1300 Ω-cm Material 40 mil Thick and Irradiated With 2 MeV Electrodes (The measurements have been made on sample # 2-9 which has been given a dose of 6.7×10^{16} cm^{-2})

Dimensions of Electrodes	V_T	V_H	V_T/V_H	R_B
500 μ x 500 μ	1200 V	180 V	6.7	400 K Ω
1000 μ x 1000 μ	1000 V	190 V	5.3	320 K Ω
1500 μ x 1500 μ	900 V	190 V	4.7	320 K Ω
2000 μ x 2000 μ	750 V	200 V	3.8	80 K Ω

clear that the smaller electrode areas result in the highest threshold voltage and lowest holding voltage.

4.5 High-Voltage Planar p-i-n Diodes

The occurrence of a negative differential resistance (NDR) region in the I-V characteristics of p-i-n diodes containing deep levels has been observed by several workers.[13-16] In this section the influence of recombination centers, introduced by electron irradiation, on p-i-n diode current-voltage characteristics is discussed. The p-i-n diodes processed for this investigation are similar to the ones we published earlier.[7]

Electrical measurements of these devices exhibited the I-V characteristics shown in Figure 12. The ac measurements show ideal diode characteristics with a blocking voltage of 5 kV, which is beyond the limit of the curve tracer used for this picture, and leakage current in the μA range. Upon electron irradiation with 2 MeV electrons to 10^{17} cm^{-2} dose, these devices showed a negative differential resistance in both forward and reverse direction. Figure 13 is a typical I-V measurement which shows a threshold voltage, V_T = 1600 volts, and holding voltage, V_H = 140 volts. Due to the continuous shift in the I-V characteristics discussed earlier, this measurement was taken as a multiple exposure using ac pulsed testing to show the values of V_T and V_H. However, when these devices were annealed at 475°C for 90 minutes in N_2 ambient, the shifting phenomenon disappeared. At the same time the threshold voltage was decreased and the holding voltage also decreased. Moreover, this display was only exhibited in the reverse direction. Figure 14 shows the ac I-V characteristics exhibiting a threshold voltage, V_T = 300 volts, with R_B = 600 ohm and, holding voltage, V_H = 50 volts, at a holding current, I_H = 1.5 amps. The influence of increasing total recombination center on the I-V characteristics has been investigated using different electron irradiation doses. Results similar to what is discussed in Table 4 have

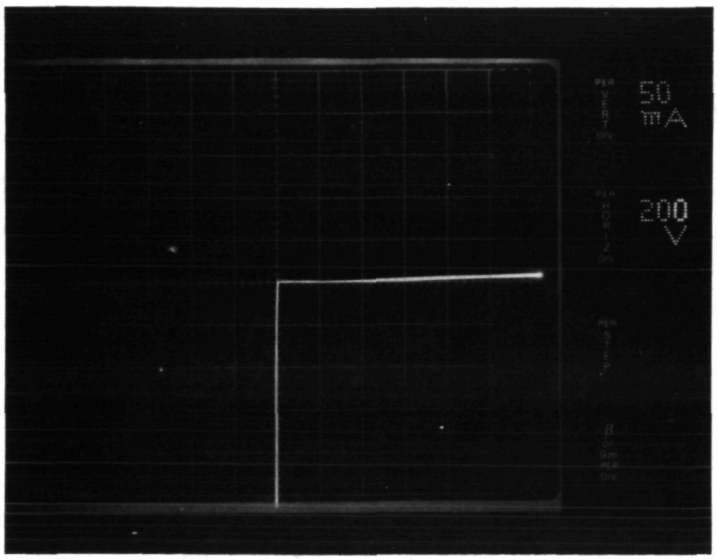

Figure 12. Reverse and forward current-voltage characteristics of a p-i-n diode before electron irradiation.

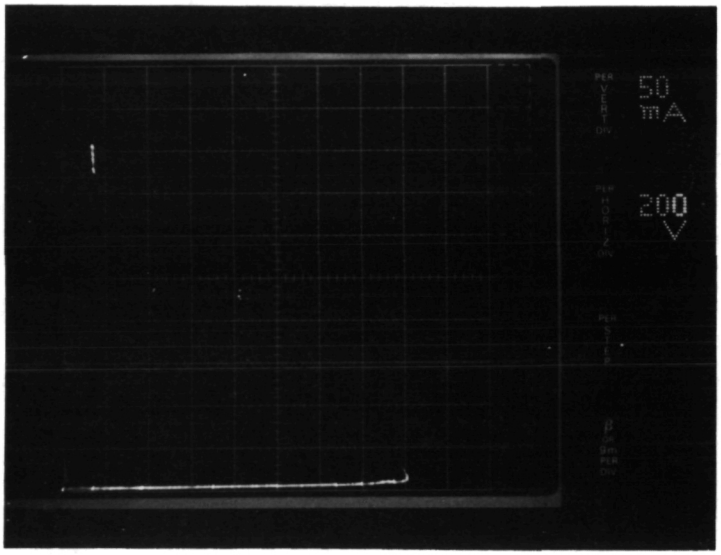

Figure 13. Reverse current-voltage characteristics of p-i-n diode after electron irradiation (forward characteristics are similar).

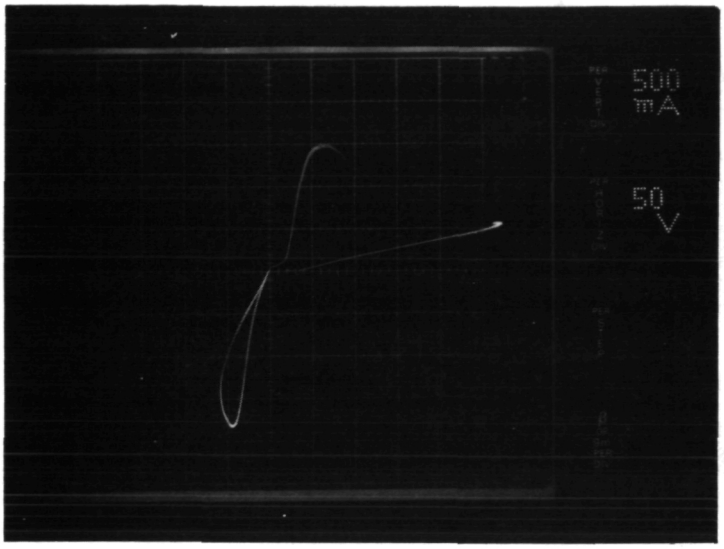

Figure 14. Reverse and forward I-V characteristics of p-i-n diode after electron irradiation and annealing.

been also observed. It is obvious that the variation of trapping center concentrations influences all the I-V characteristics with changes in V_T and V_H. This is again plausible, since the total trapping center concentration, N_t, determines the carrier lifetime and since an increasing N_t yields an increasing fixed-space charge, producing a shift of the I-V curves to higher voltages.

5. CONCLUSIONS, PROJECTIONS, AND RECOMMENDATIONS FOR FUTURE WORK

Perhaps the most important point to be conveyed here is that $(DI)^2$ devices offer real performance advantages over conventional p-n junction devices. The upper limit of power levels in these devices is not completely controlled by the p-n junction characteristics.

We have successfully demonstrated the feasibility of manufacturing $(DI)^2$ switches with 1600 volt blocking capability and 1.5 ampere holding current. Further understanding of $(DI)^2$ device physics and more optimization of design parameters will pave the way for higher power levels, decrease the "on-state" holding voltage, and increase the holding current. The dynamic switching characteristics can also be improved.

The exact nature and concentration of trapping centers required for optimum device design have not been determined. The contribution of the different n^+ and p^+ electrodes to the threshold voltage and holding voltage is not yet understood. However, the results reported for p-i-n diodes suggest the importance of these diffusions for improved device characteristics.

The work has been very successful and the results obtained represent the highest blocking voltage reported for $(DI)^2$ devices. While there are many engineering problems to be solved in realizing higher power switching performance, it is expected that further improvements will extend the power of $(DI)^2$ devices to the multi-kW to megawatt power levels.

It is hoped that these results will stimulate further investigation and future research work for careful analysis of the following tasks:

1. Optimization of electrode topology and device structures to attain specific current-voltage ratings and switching characteristics.
2. Investigations of methods and design techniques to study bulk, surface, and contact contribution to the threshold and holding voltages.
3. Development of practical methods to introduce deep levels into bulk Si as a function of base resistivity, device structure, and switching requirements.
4. Study of gold-diffusion profile and deep-center energy level requirements as a function of device-switching characteristics.
5. Methods of gating $(DI)^2$ devices and methods of electrical control of their characteristics.

It is believed that progress in solving these problems will yield the technology for a new family of semiconductor switching devices with the power level and requirements for NASA applications.

REFERENCES

1. M. A. Lampert, Proc. IRE, 50, 1781 (1962).

2. M. A. Lampert, Phys. Rev. 125, 126 (1962).

3. K. L. Ashley and A. G. Milnes, J. Appl. Phys. 35, 369 (1964).

4. Ashok K. Kapoor and H. Thurman Henderson, IEEE Electron Devices Letters, Vol. EDL-2, No. 3, March 1981.

5. P. Tuntasood, Ph.D. Thesis, University of Cincinnati (1982).

6. M. A. Lampert and P. Mark, Current Injection in Solids, Ch. 14, Academic Press, 1970.

7. F. A. Selim, IEEE, EDL-2, 219 (1981).

8. Tsay-Jiu Shieh, M. Sc. Thesis, University of Cincinnati (1983).

9. J. W. Corbett, Electron Irradiation Damage in Semiconductor and Metals, New York, Academic Press, 1966.

10. A. D. Erwaraye, J. Appl. Phys., 48, 734 (1977).

11. P. Rai-Choudhury, J. Bartko, and J. E. Johnson, IEEE Trans. Elec. Dev., ED-23, 814 (1976).

12. F. A. Selim, P. D. Blais, P. Rai-Choudhury and R. F. Yut, Semiconductor Silicon, Electrochemical Soc., Inc., NY (1977).

13. M. A. Lampert and A. Rose, Phys. Rev. 121, 26 (1964).

14. N. Holonyak, Jr., Proc. IRE 50, 2421 (1962).

15. V. V. Osipov and V. I. Stafeev, Sov. Phys. Semicond. 1, 1486 (1968).

16. R. Kassing and I. Dudeck, Phys. Status Solidi A31, 431 (1975).

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